REMARKS

Claims 1-6, 8-17, and 18-22 will be pending in the current Application upon entering this Amendment. Claims 1-6, 8, 17, and 19-21 have been amended and claim 18 has been cancelled. Applicant submits that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicant also submits that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Rejection of claims 1-6, 8-9, 12-16, and 18-22 under 35 U.S.C. 103(a)

Applicant respectfully submits that claims 1-6, 8-9, 12-16, and 18-22 are patentable over US Patent No. 5, 701, 495 (hereinafter referred to as Arndt) in view of US Patent No. 6,185,629 (hereinafter referred to as Simpson).

Claim 1

Applicant submits that claim 1, as amended, is allowable over Arndt in view of Simpson. Applicant has amended claim 1 to include "assigning an interrupt prioritization level to storage locations of the first storage device and the second storage device," which was previously a limitation of dependent claim 2. Applicant submits that neither Arndt, Simpson, nor their combination teach or suggest assigning an interrupt prioritization level as claimed in claim 1. The Examiner states that bit fields 24-31 of the XIVR register of Arndt teach or suggest this limitation; however, Applicant respectfully disagrees. Bits 24-31 allow an interrupt priority to be assigned to a particular interrupt; however, these bits do not assign an interrupt prioritization to storage locations of queues 56 and 57. That is, claim 1 requires assigning an interrupt prioritization level *to storage locations* of the first and second storage devices such that particular storage locations have a particular interrupt prioritization associated with them. Bits

24-31 within the interrupt vector register *in the IOCs* allow for specifying different priorities for specific interrupts, as needed, but does not teach or suggest assigning an interrupt prioritization level to storage locations of queue 56 or 57. Therefore, for at least those reasons, Applicant submits that claim 1 is allowable over Arndt in view of Simpson. Claims 2-6 depend directly or indirectly from allowable claim 1 and are therefore allowable for at least those reasons mentioned above with respect to claim 1.

Furthermore, claim 6 further requires changing prioritization level of a predetermined hardware-generated interrupt by providing a software-generated interrupt which represents a corresponding hardware-generated interrupt source for the predetermined hardware-generated interrupt but with a different prioritization level than the predetermined hardware-generated interrupt. Applicant submits that Arndt does not teach or suggest this limitation. For example, Arndt does not teach or suggest changing the prioritization level of a predetermined hardware-generated interrupt. That is, in Arndt, the priorities of the interrupts themselves are not changed. The interrupts are presented by the IOCs with a given priority (from the XIVR) so that they may be routed by the interrupt routing layer to a particular processor. This given priority is not changed, but is used to properly route the interrupt, i.e. to determine if the interrupt should be rejected or placed in the XIRR of a processor (see Arndt, col. 9, line 15-59). For example, if the priority of an interrupt received from an IOC is less favored or equal to the existing queued interrupts, then the interrupt is rejected. However, if it is more favored than an existing queued interrupt which has already been placed in the XIRR of the target processor, then the interrupt placed into the XIRR previously is rejected and the new interrupt takes its place. (See Arndt, col. 9, lines 34-50.) When the processor software reads the XIRR at the beginning of interrupt processing, the priority of the current processor (the CPPR value) is updated with the priority of the interrupt represented by the XISR value in order to prevent interruption with a less favored interrupt. (See col. 9, line 60 – col. 10, line 10.) Therefore, in Arndt, the priorities of the interrupts themselves are not changed. Instead, the priorities of the processor (corresponding to the level of the interrupt currently being serviced by that processor), are changed via the CPPR values in order to prevent the interrupt routing layer from interrupting the current servicing of an interrupt with a less favored interrupt. Furthermore, claim 6 does not merely claim changing a prioritization level of an interrupt, but specifically claims how a change in prioritization of a hardware-generated interrupt can be performed by providing a software-generated interrupt.

Arndt also does not teach or suggest providing a software-generated interrupt to change prioritization of a hardware-generated interrupt. Therefore, for at least those reasons stated above with respect to claim 1 and for these additional reasons, Applicant submits that claim 6 is allowable over Arndt in view of Simpson, since neither Arndt, Simpson, nor their combination teach or suggest each of the elements of claim 6.

Claim 8

Applicant submits that claim 8 is allowable over Arndt in view of Simpson because neither Arndt, Simpson, nor their combination teach or suggest each and every limitation of claim 8. For example, claim 8, which has been amended to include the limitations of dependent claim 18, claims assigning an interrupt prioritization level to storage locations of the first storage device and the second storage device. Neither Arndt, Simpson, nor their combination teach or suggest this limitation. As discussed above in reference to claim 1, bits 24-31 within the interrupt vector register in the IOCs allow for specifying different priorities for specific interrupts, as needed, but does not teach or suggest assigning an interrupt prioritization level to storage locations of queue 56 or 57. Therefore, for at least these reasons, Applicant submits that claim 8 is patentable over Arndt in view of Simpson. Claims 19-21 depend from claim 8, and are therefore allowable for at least those reasons described above with reference to claim 8.

Furthermore, claim 19 further requires assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from some interrupt sources generating hardware interrupts and having a corresponding interrupt prioritization level. Arndt, at col. 4, lines 25-32, discusses software queues which store events comprising hardware generated interrupts and software generated interrupts, but there is not teaching or suggestion of assigning a portion of the plurality of software-generated interrupt signals to represent interrupts from sources generating hardware interrupts, as claimed in claim 19. Therefore, claim 19 is also allowable over Arndt in view of Simpson for these additional reasons.

Claim 9

Applicant submits that claim 9 is allowable over Arndt in view of Simpson because neither Arndt, Simpson, nor their combination teach or suggest each and every limitation of claim 9. For example, neither Arndt, Simpson, nor their combination teach or suggest logic circuitry which determines priority between two interrupts, a first interrupt being hardware-generated and a second interrupt being software-generated, as claimed in claim 9. The Examiner agrees that Arndt does not teach or suggest this limitation, and instead cites Simpson. Simpson teaches using a round robin scheme to determine priority between multiple requests received with the same priority. However, there is no teaching or suggestion of using this round robin scheme between hardware-generated interrupts and software-generated interrupts, as claims in claim 9. Simpson discusses the round robin scheme with respect to packet transfers but does not prioritize between hardware-generated interrupts and software-generated interrupts. Therefore, for at least these reasons, Applicant submits that claim 9 is allowable over Arndt in view of Simpson. Claims 10-13 depend directly or indirectly from allowable claim 9 and are therefore allowable for at least those reasons mentioned above with respect to claim 9.

Furthermore, claim 10 further claims each of the hardware interrupt storage device and the software interrupt storage device having an assigned interrupt prioritization level to specific storage locations. Neither Arndt, Simpson, nor their combination teach or suggest this limitation, as discussed above with respect to claims 1 and 8. Also, claim 10 further claims the interrupt prioritization level of the hardware interrupt sources being permanently assigned. The Examiner cites col. 4, lines 53-61 of Arndt, however, these sections simply discusses the existence of a server number associated with each queue 42, 43. This does not teach or suggest the interrupt prioritization levels as claimed in claim 10.

Claim 14

Applicant submits that claim 14 is not anticipated by Arndt because Arndt does not teach or suggest each and every limitation of claim 14. For example, claim 14 requires executing software "to generate a predetermined software-generated interrupt signal which emulates a predetermined one of the hardware-generated interrupt sources but with a priority which differs from the predetermined one of the hardware-generated interrupt sources." However, Arndt makes no mention about using software-generated interrupt signals to emulate hardware-

generated signals. The Examiner, in the Response to Arguments section of the current Office Action, states that the implementation of the XIRR and queues 56 and 57 implies emulation; however, Applicant disagrees with this characterization. The Examiner also states on page 4 of the current Office Action that the software in Arndt "receive and read and store this value once this interrupt has been presented this will signals hardware that software will start processing this implies emulation; furthermore, software sets and removes priority which implies changing prioritization of servicing." However, this characterization is also incorrect. Emulation generally refers to the use of software to simulate a typically hardware function. That is, claim 14 requires generating a predetermined software-generated interrupt which emulates (i.e. simulates) a hardware-generated interrupt. In Arndt, the software reads and writes to the XIRR in order process interrupts and to determine whether the XIRR should be updated with a more favored interrupt (as discussed in more detail above with respect to claim 6). However, there is no teaching or suggestion of actually *generating a software-generated interrupt to emulate* or simulate a hardware-generated interrupt but with a different priority. Furthermore, as described above in reference to claim 6, Arndt does not teach or suggest changing the priority of an interrupt. Simply the use of software to accept/reject interrupt requests or to service requests, as discussed in the sections of Arndt cited by the Examiner, does *not* imply emulation. Furthermore, simply using software to change the priority of an interrupt does not imply emulation. Therefore, for at least these reasons, Applicant submits that claim 14 is allowable over Arndt in view of Simpson. Claims 15 and 16 depend directly or indirectly from claim 14 and are therefore allowable for at least those reasons described above in reference to claim 14.

Claim 22

Applicant submits that claim 22 is not anticipated by Arndt because Arndt does not teach or suggest each and every limitation of claim 22. For example, claim 22 requires changing prioritization level of a predetermined hardware-generated interrupt by providing a software-generated interrupt which represents a corresponding hardware-generated interrupt source for the predetermined hardware-generated interrupt but with a different prioritization level than the predetermined hardware-generated interrupt. Applicant submits that Arndt does not teach or suggest this limitation. As discussed above with respect to claim 6, Arndt does not teach or

suggest changing the prioritization level of a predetermined hardware-generated interrupt. That is, in Arndt, the interrupts are presented by the IOCs with a given priority (from the XIVR) so that they may be routed by the interrupt routing layer to a particular processor. This given priority is not changed, but is used to properly route the interrupt, i.e. to determine if the interrupt should be rejected or placed in the XIRR of a processor (see Arndt, col. 9, line 15-59). When the processor software reads the XIRR at the beginning of interrupt processing, the priority of the current processor (the CPPR value) is updated with the priority of the interrupt represented by the XISR value in order to prevent interruption with a less favored interrupt. (See col. 9, line 60 – col. 10, line 10.) Therefore, in Arndt, the priorities of the interrupts themselves are not changed. Instead, the priorities of the processor (corresponding to the level of the interrupt currently being serviced by the processor), are changed via the CPPR values in order to prevent the interrupt routing layer from interrupting the servicing of an interrupt with a less favored interrupt. Furthermore, claim 22 specifically claims how a change in prioritization of a hardware-generated interrupt can be performed by providing a software-generated interrupt. Therefore, for at least those reasons stated above and with respect to claim 6, Applicant submits that claim 22 is allowable over Arndt in view of Simpson, since neither Arndt, Simpson, nor their combination teach or suggest each of the elements of claim 22.

Conclusion

Although Applicant may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicant is not discussing all these statements in the current Office Action, yet reserves the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 502117.

Respectfully submitted,

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